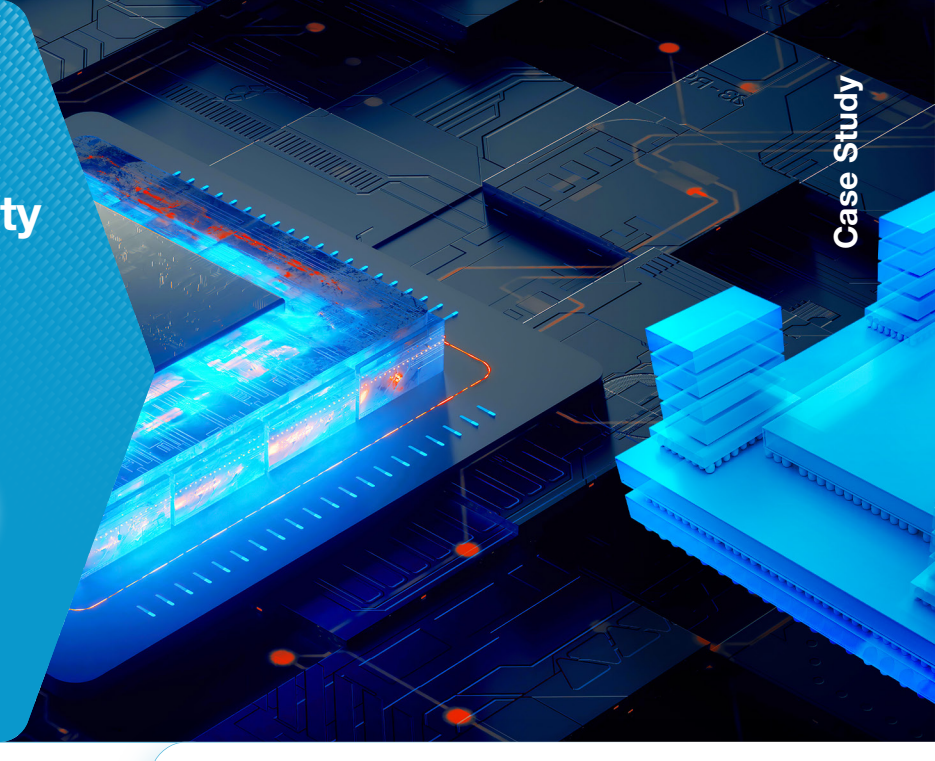
proteanTecs

Datacenter Chipmaker Achieves 2.5D SOC Reliability with 100% Interconnect Coverage

Case Study

Explore the fabless chipmaker's quality leap thanks to die-to-die interconnect failure prediction based on parametric lane grading



REDUCED 502 DPPM
Defective Parts per Million

SAVED >$250K
Cost of further testing of affected dies

SAVED >$1M
Cost of recall & RMA investigation

The Customer

A fortune-100 chipmaker designing 5nm datacenter chiplets

The customer develops chiplet-based AI SOCs for server farms.

The advanced packages, 2.5D ICs, incorporate multiple dies to overcome the limitations of silicon manufacturing.

Breaking the design into smaller chiplets has multiple benefits, such as improving yield and combining dies manufactured in different processes.

The Challenge

Quality issues due to poor visibility of the die-to-die (D2D) interconnects

In advanced heterogeneous packages, only a fraction of the internal pins that connect the chiplets are accessible to the test program. Even if the individual dies undergo thorough testing, the thousands of lanes between them remain in the dark.

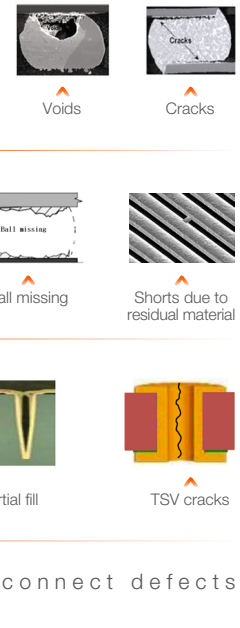
This presents a severe quality risk and interconnect defects can pass undetected as false positives.

Several factors contribute to poor visibility in D2D interfaces:

Low lane coverage → High risk of failure

Mere pass/fail results → Undetectable marginal performance

No in-mission monitoring → Unpredictable field quality



D2D interconnect defects

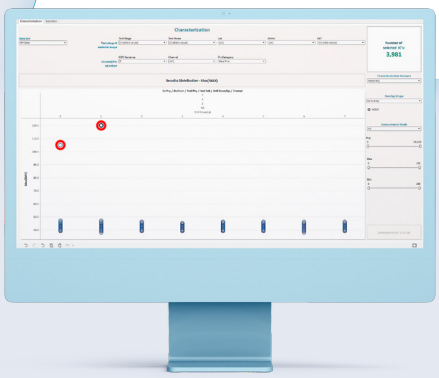
The Solution

Interconnect failure prediction with 100% coverage

The customer embedded proteanTecs D2D interconnect monitoring solution to improve the advanced package quality. It includes a deep data analytics platform that grades each lane based on parameters from dedicated on-chip Agents.

The solution offers parametric lane grading with 100% coverage, leading to the detection of small and marginal defects, that would have made it to the field as "walking wounded" devices.

Outliers detected by the solution allowed the customer to swap flagged lanes with spare ones or discard faulty units that would otherwise pass all tests.



Outliers in red represent lanes with marginal performance
(Y-axis indicates the electrical eye - The higher the worse)

The Results

Substantial quality improvement: Thanks to the proteanTecs solution, the customer reduced **502 DPPM** and established reliable interconnect testing that was previously beyond reach.

Considerable cost saving: Early detection led to direct savings of over **$250,000** by preventing further testing of affected devices. The customer also saved over **$1,000,000** by avoiding RMA costs and prolonged investigations at a much later stage.later stage.

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